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EXAMINER	
FOWLKES, ANDRE R	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,774	ROBISON, ARCH D.	
	Examiner	Art Unit	
	Andre R. Fowlkes	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed 2/3/05.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-28 rejected under 35 U.S.C. 102(b) as being anticipated by Cooper, et al., (Cooper), "Enhanced Code Compression for Embedded RISC Processors", SIGPLAN '99.

As per claim 1, Cooper discloses a method comprising:

- identifying a plurality of fork subgraph structures within a graph structure constructed for a plurality of executable instructions (p. 143 col. R:23-24, "we first use the interference graph to (identify a plurality of fork subgraph structures with in a graph structure constructed for a plurality of executable instructions)"),

- identifying a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)",

and p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)"),

- transferring at least one unifiable instruction of said plurality of executable instructions from a fork of a corresponding fork subgraph structure of said plurality of fork subgraph structures to a handle of said corresponding fork subgraph structure (p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are merged together (in the handle)"),

- said at least one unifiable instruction containing at least one unifiable variable of said plurality of unifiable variables (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)").

As per claim 2, the rejection of claim 1 is incorporated and further, Cooper discloses that identifying said plurality of unifiable variables further comprises:

- constructing an interference graph structure for a plurality of local variables within said each fork subgraph structure (p. 143 col. R:23-24, "we first (construct and) use the interference graph),

- said plurality of local variables including said plurality of unifiable variables (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)"),

- identifying said plurality of unifiable variables as variables having overlapping live ranges within said interference graph structure (p. 143 figure 8, Live range analysis, and associated text (e.g. p. 143 col. L:34 – p. 144 col. R:42).

As per claim 3, the rejection of claim 2 is incorporated and further, Cooper discloses that **said interference graph structure indicates which variables of said plurality of local variables are simultaneously used in said plurality of executable instructions and cannot be unified** (p. 143 figure 8, Live range analysis, and associated text (e.g. p. 143 col. L:34 – p. 144 col. R:42), and p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)").

As per claim 4, the rejection of claim 1 is incorporated and further, Cooper discloses that identifying said plurality of unifiable variables further comprises: **constructing a data dependence** analysis **for said plurality of executable instructions; and identifying said plurality of unifiable variables using said data dependence** analysis (p. 148 col. L:57-58, "(unifiable variables are identified) subject to (data) dependence constraints").

As per claim 5, the rejection of claim 1 is incorporated and further, Cooper discloses **initializing a flag for said at least one unifiable instruction; and unifying**

each unifiable variable within said at least one unifiable instruction (p. 140 col. L:8-9, "our compression framework first identifies (i.e. flags) repeats (i.e. unifiable variables/instructions)", and p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are merged together (in the handle)").

As per claim 6, the rejection of claim 5 is incorporated and further, Cooper discloses **removing said at least one unifiable instruction from subsequent forks of said corresponding fork subgraph structure** (p. 141 col. R:27-29, "identical regions (i.e. unifiable instructions) that end with a jump to the same target (are removed from a fork) are merged together (in the handle)").

As per claim 7, the rejection of claim 4 is incorporated and further, Cooper discloses that **said data dependence** analysis **contains a plurality of dependence arcs, each dependence arc connecting two instructions of said plurality of executable instructions contained within said fork of said corresponding fork subgraph structure** (p. 148 col. L:57-58, "(unifiable variables are identified) subject to (data) dependence constraints").

As per claims 8-14, this is a system version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or

cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors (p. 140 col. L:7-18 and Figs. 3 & 4).

As per claims 15-21, this is a computer readable medium version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors (p. 140 col. L:7-18 and Figs. 3 & 4).

As per claims 22-28, this is another system version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors (p. 140 col. L:7-18 and Figs. 3 & 4).

Response to Arguments

4. Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) Cooper does not teach constructing the kind of graph that can be used to identify fork subgraphs, at p. 13:16-14:2.

Examiner's response:

1) The examiner disagrees with applicant's characterization of the applied art. Cooper does disclose constructing the kind of graph that can be used to identify fork subgraphs as evidenced by p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are (identified, then) merged together (in the handle)".

In the remarks, the applicant has argued substantially that:

2) Cooper does not teach "identifying a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions", as required by claim 1, at p. 14:3-6.

Examiner's response:

2) The examiner disagrees with applicant's characterization of the applied art. Cooper does disclose identifying a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions, as evidenced by p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)", and p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)".

In the remarks, the applicant has argued substantially that:

3) Cooper does not teach "transferring at least one unifiable instruction of said plurality of executable instructions from a fork of a corresponding fork subgraph structure of said plurality of fork subgraph structures to a handle of said corresponding fork subgraph structure", at p. 14:13-18.

Examiner's response:

3) The examiner disagrees with applicant's characterization of the applied art. Cooper does not teach transferring at least one unifiable instruction of said plurality of executable instructions from a fork of a corresponding fork subgraph structure of said plurality of fork subgraph structures to a handle of said corresponding fork subgraph structure, as evidenced by p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are merged together (in the handle)".

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571) 272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ARF

TUAN DAM
SUPERVISORY PATENT EXAMINER